Amendments to the Specification

Please replace the paragraph beginning on page 5, line 15, with the following amended paragraph:

Referring to Fig. 4, there is shown a thin film transistor substrate in a liquid crystal display (LCD) according to a first embodiment of the present invention. The LCD includes thin film transistors 6 positioned at intersections between data lines 2 and gate lines 4, pixel electrodes 14 connected to drain electrodes 12 of the thin film transistors 6, and gate dummy patterns 30 overlapping with the data lines 2 and the pixel electrodes 14 adjacent to the data lines 2. The thin film transistor 6 has a gate electrode 10 connected to the gate line 4, a source electrode 8 connected to the data line 2, a drain electrode 12 connected, via a first contact hole 16, to the pixel electrode 14, and a semiconductor layer (not shown) for providing a conductive channel between the source electrode 8 and the drain electrode 12 by virtue of a gate voltage applied to the gate electrode 10. Such a thin film transistor 6 responds to a gate signal from the gate line 4 to selectively apply a data signal from the data line 2 to the pixel electrode 14. The pixel electrode 14 generates a potential difference from a common transparent electrode (not shown) provided at the upper substrate by a data signal applied via the first contact hole 16. By virtue of this potential difference, a liquid crystal positioned between the thin film transistor substrate and the upper substrate is rotated by its dielectric anisotropic property and a light applied, via the pixel electrode 14, from a light source is transmitted into the upper glass substrate. A storage capacitor 18 provided between the pixel electrode 14 and the gate line 4 at the previous stage plays a role to prevent a voltage variation in the pixel electrode 14 by charging a voltage in a period at which a gate high voltage is applied to the previous-stage gate line 4 and discharging the charged voltage in a period at which a data signal is

applied to the ~~pixel~~ source electrode ~~14~~ 8. The storage capacitor 18 is defined by a storage electrode 20 electrically connected, via a second contact hole 22 formed in a protective film 28, to the pixel electrode 14 and a gate electrode 4 having a gate insulating layer 26 therebetween. The storage electrode 20 is formed on the gate insulating layer 26 upon formation of the data line 2 and the source/drain electrode 8 and 12. The gate dummy pattern 30 overlaps with the data line 2 and the adjacent pixel electrode 14 to serve as a black matrix as well as to perform a repair function upon break of the data line. For instance, the gate dummy pattern 30 is electrically connected to a broken data line 2 by a laser welding technique upon break of the data line 2 to permit a repair. Also, the gate dummy pattern 30 is positioned in such a manner to overlap, by about 0.5 to 1μm, with the data line 2 and the pixel electrode 14, thereby serving as a black matrix for shutting off a light leaked between the data line 2 and the pixel electrode 14. When the gate dummy pattern 30 is used as a black matrix as mentioned above, an area overlapping with the pixel electrode 14 can be more reduced in comparison to the conventional black matrix to expect an aperture ratio increase of about 5 to 6%. To this end, the gate pattern 30 is formed on a lower substrate 24 with having the gate insulating layer 26 at each side of the data line 2 as shown in Fig. 5. This gate dummy pattern is made from the same material (e.g., Al, Mo, Ti, W, Cr or Cu) as the gate line and the gate electrode. Such a gate dummy pattern 30 may be provided at both sides of the data line 2 or at one side of the data line 2. If the gate dummy pattern 30 is electrically connected to the gate line 4, then it can be used as a storage electrode forming the storage capacitor along with the pixel electrode 14 overlapped with having the gate insulating layer 26 and the protective film 28 therebetween. In this case, a capacitance value of the storage capacitor caused by the gate dummy pattern 30 is added to

the conventional storage capacitor 18, so that a voltage of the pixel electrode 14 can be maintained at more stable state.